WHAT IS CLAIMED IS:

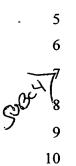
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ري	' 1		1. A method for pulse width modulation comprising the steps of:
ŹV	2/		providing a pulse width modulator having n bits of resolution and a nominal
Y /	3	time period Pn	;
(4		supplying an additional timer to generate K associated states and having a
	5	timer period P	т;
	6		associating a modulator output value with each one of said K states; and
	7		establishing a pulse width modulation update interval of K*P _T .
	1		2. The method of claim 1 wherein P_T is an integer multiple of P_n .
	1		3. The method of claim 1 wherein said pulse width modulator includes an
Ö	2	overflow bit.	
	1	(4. The method of claim 1 wherein P _T - P _n .
n	1 63		A method for improving the resolution of an n bit pulse width
	2	modulator hav	ring a nominal time period of P _n , the method comprising the steps of:
	3 C	X	supplying an additional timer having K associated states and a timer period of
U	4	P _T ;	
==== ======	5		associating a modulator output value with each one of said K states; and
	6		outputting a pulse according to said modulator output value during each time
	7	period P _n occu	arring within said timer period P _T during each one of said K timer states,
	8	whereby the re	esolution of said n bit pulse width modulator substantially equals $n = \log_2(K)$.
	1		6. The method of claim 5 wherein P_T is an integer multiple of P_n .
ks.	1	overflow bit.	7. The method of claim 5 wherein said pulse width modulator includes an
w	4	OVERTION OIL.	

The method of claim 5 wherein $P_T = P_n$.

1	9. The method of claim 5 where P_T is other than an integer multiple of
2	P_n and $P_T >> P_n$.
1	10. The method of claim 9 wherein said pulse width modulator includes an
727	overflow bit.
y ¹ 3	(11.) A computer program product for pulse width modulation comprising:
4	a computer readable storage medium having computer readable
5	program code means embedded in said medium, said computer readable program code means
6	having:
9 7	a first computer instruction means for associating K timer states with a
5 8	timer having a period P _T ; and
9 110	a second computer instruction means for reading a commanded pulse
110	width modulation duty cycle;
` <u>.</u> []11	a third computer instruction means for assigning an n bit modulator
12	output value with each one of said K states according to said duty cycle.
12 1 1 2	12. The computer program product of claim 11 wherein said third
[™] 2	computer instruction means updates said n bit modulator output value assigned to each state
3	at time intervals of K*P _T .
1	13. A method for controlling the brightness of a display using pulse width
2	modulation comprising the steps of:
3	receiving a commanded brightness level;
4	using an n bit pulse width modulator to assert a plurality of pulses in
5	accordance with an output of said n bit pulse modulator wherein said modulator has a period
6	P_n ;
7	assigning a modulator output value to each one of K states of a K state timer
8	wherein said timer has a period P/;
9	outputting said plurality of pulses according to said modulator output value
10	during each P _n period occurring within timer period P _T ; and
11	supplying power to the display in accordance with said plurality of pulses.

1	14. An apparatus for pulse width modulation comprising:
2	an n bit pulse width modulator having a nominal modulator period P_n ;
3	a timer to generate K timer states and having a timer period P_T ;
4	a computing device for assigning a modulator output value to each of said K
_5	states; and
4	whereby said modulator outputs a plurality of pulses according to said
7	modulator output value during each P_n period occurring within timer period P_T and whereby
8	said pulse width modulator has a resolution of $n + \log_2 K$.
1	15. The apparatus of claim 14 wherein said timer is included within said
2 	computing device.
	16. The apparatus of claims 14 where P_T is an integer multiple of P_n .
1	17. The apparatus of claim 14 wherein P_T is other than an integer multiple
	of P_n and $P_T >> P_n$.
_ 1	18. The apparatus of claim 4 wherein said modulator further comprises
5 1 5 2 1 1 5 1	overflow bit.
1	19. An apparatus improving the resolution of an n bit pulse width
2	modulator having a P_n period, the apparatus comprising:
3 .	a timer to generate K timer states and having a timer period P_T ;
4	a computing device for assigning a modulator output value to each of said K
5	states; and
6	whereby said modulator outputs a plurality of pulses according to a modulato
7	output value during each P_n period occurring within timer period P_T and whereby the pulse
8	width modulator has a resolution of $n + \log_2 K$.
1	20. An Land D backlit display comprising:
2	an array of LEDs;
3	an n bit pulse width modulator having a period of P_n ;



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states; whereby said modulator outputs a plurality of pulses according to said modulator output value during each P_n period occurring within timer period P_T and whereby said pulse width modulator has a resolution of $n + \log_2 K$.; and a driver for supplying power to said array in accordance with said modulator output.

a computing device for assigning a modulator output value to each of said K